Operator’s Manual

Electronic Circuit to Mimic the Neural Network for the Saccade Controller

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Project 12

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Safety Instructions

- Ensure wires are being attached to the corresponding sockets on the neuron PCBs.
- No DC voltages should be used that exceed an absolute magnitude of 15 V.
- Under no circumstances should the device be connected to anything other than proper power supplies, function generators, or signal observation devices (i.e. NI DAQ hardware, oscilloscopes, etc.).
- Ensure that the workspace is clean and dry prior to use of the device or any of its components.
- Ensure the device and any corresponding components are stationed in such a way that they cannot be knocked off of the work surface.
- Ensure all equipment is properly grounded prior to use.
- Avoid handling the PCBs unless it is necessary.
  - If handling the boards becomes necessary, discharge any static electricity built up prior to touching the boards.
- If there is any suspicion that part of the device has malfunctioned or broken during use, turn off the power sources and allow at minimum 30 seconds for the device to discharge before any portion is manipulated.
- If the device, or any of its PCB components are dropped, check all solder joints and wires thoroughly for any damage. Replace broken parts or joints as needed.

**Signs that the device may be malfunctioning or damaged:**
- Sudden, dramatic rise in temperature of any portion of the circuitry
- Sparks emitting from any portion of the circuitry
- Smoke rising from any portion of the circuitry
- Popping noises coming from any portion of the device
- Sudden disruption of any signals being obtained
- Increased system noise
- Unexpected signal amplification or dampening

If any of these scenarios have occurred, turn off the power supplies and other devices connected to the circuitry. Allow at minimum 30 seconds for the system to dissipate any stored energy, then troubleshoot only if the situation is safe.
Parts and Accessories

Neuron Circuits

**Neuron PCB:** For more specific identification, please observe acronym label on the board.

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>SC</td>
<td>Superior Colliculus</td>
</tr>
<tr>
<td>FN</td>
<td>Fastigial Nucleus</td>
</tr>
<tr>
<td>LLBN</td>
<td>Long-Lead Burst Neuron</td>
</tr>
<tr>
<td>EBN</td>
<td>Excitatory Burst Neuron</td>
</tr>
<tr>
<td>TN</td>
<td>Tonic Neuron</td>
</tr>
<tr>
<td>OPN</td>
<td>Omnipause Neuron</td>
</tr>
<tr>
<td>IBN</td>
<td>Inhibitory Burst Neuron</td>
</tr>
<tr>
<td>AN</td>
<td>Abducens Nucleus</td>
</tr>
<tr>
<td>ON</td>
<td>Oculomotor Nucleus</td>
</tr>
</tbody>
</table>

**Dendrite**

**Synapse**  **Axon Post-Processor**  **Axon**  **Current Stop**
Possible Accessories (Actual devices may vary in appearance)

**Power Supply**: Produces constant DC voltage signals.

**Oscilloscope**: Uses probes to measure electrical signals.

**Function Generator**: Used to stimulate a neuron or neural network.
Features

The nature of this device causes there to be limited interaction between the device and the user. Much of the work associated with its design and fabrication is based off of theoretical simulation and physiological modeling concepts. As a result, the operation of the device is straightforward in terms of device manipulation, but the interpretation of the data requires some background in the behavior of the neural network for the saccade controller.

A notable piece of behavior for the device that may be considered unexpected occurs when the device is first powered on. Due to the behavior of some of the circuits, particularly the dendrite components, there is a delay between the instant the device is turned on and when it has reached steady state, the point at which it is ready for use. Figure A shows the dendrite and axon voltage signals of a neuron that is undergoing this initial transition to steady state. This process, in its entirety, is quite brief, though allowing the system to stabilize for the first few seconds of operation will ensure that the neurons function properly once stimulated.

Figure A: The dendrite (green) and axon (red) voltage signals immediately after the device is powered on. This behavior is the result of the system attempting to reach steady state.
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1 Introduction

1.1 Overview

The Electronic Circuit to Mimic the Neural Network for the Saccade Controller comprises a collection of NI Multisim simulation files as well as a less complete physical prototype. The operation of both will be described.

Multisim Model

In order to simulate the entire system with NI Multisim, it had to be split into ten pieces that must be run in order. These simulations are important for demonstration and testing purposes. Each piece is an .ms11 file that contains section of the neural network described in A Third Order Linear Saccade Model by Enderle and Zhou. File names indicate the order in which the simulations should be run. Table 1 outlines the contents of each simulation file.

<table>
<thead>
<tr>
<th>File Name (*.ms11)</th>
<th>Neurons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Demonstration Part 1</td>
<td>SC &amp; LLBN (left and right)</td>
</tr>
<tr>
<td>Demonstration Part 2</td>
<td>OPN</td>
</tr>
<tr>
<td>Demonstration Part 3</td>
<td>EBN (right)</td>
</tr>
<tr>
<td>Demonstration Part 4</td>
<td>IBN (right)</td>
</tr>
<tr>
<td>Demonstration Part 5</td>
<td>EBN (left)</td>
</tr>
<tr>
<td>Demonstration Part 6</td>
<td>IBN (left)</td>
</tr>
<tr>
<td>Demonstration Part 7</td>
<td>TN (right)</td>
</tr>
<tr>
<td>Demonstration Part 8</td>
<td>TN (left)</td>
</tr>
<tr>
<td>Demonstration Part 9</td>
<td>AN &amp; ON (right)</td>
</tr>
<tr>
<td>Demonstration Part 10</td>
<td>AN &amp; ON (left)</td>
</tr>
</tbody>
</table>

Table 1. A list of the demonstration files and the neurons contained within each.

A demonstration file is an environment in which neurons are simulated. Power supplies and signal routing are set up in these files. Neurons, however, are self-contained Multisim files that are imported as hierarchical blocks into the demonstration file. As a hierarchical block, neurons have open ports for power supplies, inputs, and outputs that are connected appropriately in the demonstration file.

A given demonstration file is kept in a folder with its accompanying neurons to ensure proper operation when moving between computers. Neurons and sets of demonstration files are assigned version numbers, with minor changes advancing the number by 0.1 and major advancements advancing it by 1.0 or more. A major change also calls for a new codename, for which the convention is “[Adjective] [Fruit] [Dessert]”, i.e. “LLBN 6.2 - Delightful Raspberry Tart”.

In general, running a demonstration involves using a LabVIEW Text-based Measurement File (.LVM) as a voltage input and saving a file of the same type as an output once the simulation is run. Step-by-step instructions for this will be given in the proceeding section.
The Neuron

With the exception of the tonic neuron, which has an additional integrator circuit, neurons are identical except for changes in component values. The three major parts of the neuron circuit are the dendrite, axon, and synapse, and are shown in Fig. 1.

![Neuron Circuit Diagram](image)

Figure 1. The main sections of the neuron circuit are the dendrite, axon, and synapse. The black squares are bus connectors that correspond to ports on the outside of the hierarchical block.

Table 2 describes the purpose of each connector.

<table>
<thead>
<tr>
<th>Connector</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iin</td>
<td>The input signal to the neuron; from a current source.</td>
</tr>
<tr>
<td>Dend</td>
<td>Observation point for dendrite membrane voltage.</td>
</tr>
<tr>
<td>Axon</td>
<td>Observation point for axon membrane voltage.</td>
</tr>
<tr>
<td>EVout</td>
<td>Excitatory output from neuron; a voltage; fed into summer and current source.</td>
</tr>
<tr>
<td>IVout</td>
<td>Inhibitory output from neuron; a voltage; fed into summer and current source.</td>
</tr>
<tr>
<td>+15V</td>
<td>Must be connected to a positive 15-Volt source; for operational amplifiers in the dendrite current stop, axon post-processing, and synapse.</td>
</tr>
<tr>
<td>-15V</td>
<td>Must be connected to a negative 15-Volt source for reasons stated above.</td>
</tr>
<tr>
<td>Vrp</td>
<td>Resting potential voltage in the dendrite; must be connected to a -60 mV source.</td>
</tr>
<tr>
<td>+2V</td>
<td>Must be connected to a positive 2-Volt source for synapse comparator operation.</td>
</tr>
<tr>
<td>-0.4V</td>
<td>Must be connected to a negative 0.4-Volt source for axon operation.</td>
</tr>
<tr>
<td>GND</td>
<td>The overall ground for the circuit; must be connected to the ground. The outside of the cell membrane is designated as ground.</td>
</tr>
</tbody>
</table>

Table 2. The connectors found in the simulation and their purposes are described.

Dendrite
The dendrite acts as a passive filter. Charge passively flows along it, and small disturbances that are not desirable signals are filtered out. The three types of dendrite compartment: the first, intermediate, and soma, differ only in their number of axial resistors. Fig. 2 shows what is inside the dendrite block seen in Fig. 1. Fig. 3 shows the three types of dendrite compartment.

Figure 2. An overview of the dendrite is shown. Three types of compartments are present, as well as the current stop.

Figure 3. The three types of dendrite compartment, from left to right, are the first, intermediate, and soma, respectively. The intermediate compartment is repeated nine times, giving eleven compartments in total.

The soma is followed by the current stop, which is used to isolate the dendrite from reverberations from the axon, as well as to amplify the stimulation of the axon. The current stop is shown in Fig 4.

Figure 4. The current stop is shown. The circuit serves to subtract the -60 mV resting potential from the signal to obtain a zero-baseline, and to amplify the voltage such that it is appropriate for stimulating the axon circuit. The operational amplifiers and diode prevent current from flowing from the axon to dendrite.

Note that the red X on a power supply pin indicates that the operational amplifier is already supplied because a multi-amplifier chip is being used. A technical description of each
component, including how to change time constants and how to adjust firing thresholds and rates, is given in section three.

Axon

The axon block of Fig. 1 contains a FitzHugh-Nagumo oscillator representing the axon hillock and a post-processing unit to scale and shift the oscillator's output to physiologically appropriate levels. The arrangement of these components is shown in Fig. 5.

![Axon circuit diagram](image1)

Figure 5. An overview of the axon circuit is shown.

The FitzHugh-Nagumo oscillator used to model the axon hillock is shown in Fig. 6. This circuit produces action potentials when stimulated with a direct current. The frequency of action potentials is proportional to this current.

![FitzHugh-Nagumo oscillator diagram](image2)

Figure 6. The implemented FitzHugh-Nagumo oscillator is shown.

The axon post-processing unit is shown in Fig. 7. The circuit scales and shifts the action potentials produced by the FitzHugh-Nagumo oscillator. Because of its simplicity, the oscillator has a resting value of 0V and produces action potentials of around 5V amplitude. The post-processing unit scales the action potential amplitude to a realistic value of 100mV and shifts resting potential to -60mV.

The post-processing circuit is purely for observation and recording; the non-scaled output of the axon hillock, the “OUT” pin, is fed directly to the synapse.
Figure 7. The axon post-processing circuit is shown. It adds a resting potential to a scaled axon output to create a signal that is within a physiological voltage range.

An in-depth description of the axon is provided in section three.

**Synapse**

The synapse circuitry creates an input current to the next neuron that is proportional to the frequency of action potentials produced by the axon hillock. Inside the “Synapse” block of Fig. 1 is the circuitry representing the presynaptic terminal. This is shown in Fig. 8.

Figure 8. The presynaptic terminal circuitry comprises a comparator and an inverting amplifier.

The comparator and inverting amplifier are shown in Fig. 9.

Figure 9. The comparator, left, and inverting amplifier, right, are shown.
The comparator simply takes the non-scaled action potentials as input and creates a positive square pulse per action potential. This output is used to generate current to excite a postsynaptic neuron. If inhibition is desired, the output is run through an inverting amplifier to create negative pulses. Both inhibitory and excitatory outputs are provided in the model, representing inhibitory and excitatory neurotransmitter, respectively.

The generation of a postsynaptic potential is modeled as a summation of the inhibitory and excitatory effects of all presynaptic neurons converted into a current that is injected into the postsynaptic dendrite. The block shown in Fig. 10 is found in demonstration files preceding any neuron that has multiple inputs.

![Figure 10](image1.png)

Figure 10. The voltage summer and current source accepts multiple inputs from presynaptic terminals and outputs an input current for the postsynaptic neuron.

The circuit inside this block is shown in Fig. 11.

![Figure 11](image2.png)

Figure 11. The contents of the voltage summing and current block are shown. It comprises an inverting summing amplifier and bilateral current source.

The resistors of the summing amplifier may be manipulated to achieve different relative synaptic strengths. The current source may also be manipulated, but it is inconvenient and unnecessary.

It is important to note that the sign of the current leaving the current source is opposite to that of the voltage at its input. A more thorough description is provided in section three.

**Prototype**

Each neuron is contained on a printed circuit board. A 3-D model of a neuron is shown in Fig. 12.
In the complete prototype, a central circuit board will take care of the routing, observation points, and power supply provisions, much like the demonstration files for running the Multisim models. The neurons will be connected to the central board with ribbon cable via 24-pin ports.

One such port is seen at the top of Fig. 12. Each pin in Table 1 is represented in the port, and the pin mapping is discussed in section three. Testing the neuron without the central board would involve contacting the pins directly and generating voltages with external power supplies. A function generator may then be used to create an input current.

1.2 Step-by-Step Instructions

The first demonstration file contains the current sources representing the superior colliculi and the left and right LLBN models. A full view of the first demonstration file is shown in Fig. 13.
Figure 13. The first Multisim demonstration file is shown.

It is crucial that the demonstration file be in a folder with the individual neuron files. The neuron files are imported into the demonstration as a hierarchical block. The voltage ports on the neuron block are supplied for proper function, and all operational amplifiers must be checked for proper supply voltage connections before running the model.

Mishaps occur when operational amplifiers are renamed and stripped of their supply voltages. Thus, to ensure supply voltages are correct, make sure current stop, axon post-processing units, and voltage summing blocks contain operational amplifiers of the same number, labeled A through D.

One may select a time and length for a saccade by changing the properties of the superior colliculus current sources, but the default is a 20 millisecond pulse of 10 µA initiating in the left superior colliculus. The current probe attached to each superior colliculus converts current to voltage for viewing on an oscilloscope, and its conversion ratio is set such that 0 – 10 µA appear are 0 – 15 Volts. The settings for the left superior colliculus are shown in Fig. 14 and the current probe settings are shown in Fig. 15.
Figure 14. The default left superior colliculus settings are shown. The delay time parameter sets when the pulse occurs, and the pulse width parameter determines its length.

Figure 15. The superior colliculus current probe default settings are shown.

To operate the demonstration, the simulation is run for a period of time that allows for all activity to take place; 400 milliseconds should suffice. The oscilloscopes attached to the pins labeled “Axon” and “Dend” show physiologically accurate axon and dendrite membrane voltage, respectively. The pins labeled “EVout” and “IVout” output synaptic pulses of voltage between 0 and ±15 Volts that are used to excite or inhibit the next neurons.

The synaptic output simulation data should be saved in the .LVM file format by pressing the “Save” button within the oscilloscope window, highlighted in Fig. 16.
Figure 16. The oscilloscope window with simulation data and “Save” button highlighted is shown. The subset shows the appropriate file format for saving data.

The default options in the second dialog are satisfactory. The simulation data from the “Axon” and “Dend” pins may be saved under a different name or location for viewing in parallel with a LabVIEW VI.

The next demonstration file is opened when the required simulation data is saved. The second file is shown in Fig. 17.

Figure 17. The second demonstration file is shown.
The .LVM files from the synaptic outputs of the LLBNs in the previous files are used as inputs for the .LVM controlled voltage sources seen in the left side of Fig. 17. Set the file path to the .LVM file by double-clicking the voltage source.

Besides file location, the default voltage source options are acceptable, as the appropriate synaptic output was attached to channel A in the previous file. The same steps are repeated for the subsequent demonstration files, saving synaptic outputs and using them as voltage sources for the appropriate post-synaptic neurons in the proceeding files. These steps effectively bridge the gap between Multisim files and allow for the network to be run in increments.

The basic LabVIEW VI called “Neuron View” may be used to view the axon and dendrite voltages over time after running all parts of the simulation. Simply run the program, and select the appropriate .LVM file that is displayed on the button in the bottom right corner. The graphs on the front panel will then be populated with simulation data.
2 Maintenance

2.1 Multisim Files

The Multisim files should require no maintenance from the user. It is recommended that a permanent copy of the demonstration files be kept in case the device they are stored on (computer hard drive, flash drive, etc.) is damaged such that the files may not be retrieved. This will also allow for a failsafe in case any modifications are made to the demonstration files (intentional or unintentional) that cause them to malfunction.

Beyond file backup, the only other maintenance regarding this portion of the product would be to follow the recommended maintenance guidelines for the device running the demonstration files. This can include, but is not limited to, running and maintaining antivirus software, keeping up-to-date versions of NI Multisim and NI Ultiboard, and proper care for the computer components.

2.2 Prototype

The components of the prototype were designed such that minimal maintenance would be required. However, there are several aspects of each part of the testing setup that should be checked prior to any simulations being performed.

General guidelines for all portions of the prototype include storage in a location that will not be prone to excessive heat or cold. The neuron circuits are designed to function at least up to 90˚F, though the functional temperature ranges for other components should be determined from the documentation supplied with each. Avoiding particular humid environments would also help protect against short-circuiting of the various parts of the testing setup.

Surface cleaners are usable on the device (unless otherwise noted), though cleaners using corrosive chemicals should be avoided. Recommended cleaners would be those with an alcohol base, allowing for quick evaporation and no residue.

Neuron Circuit Boards

The PCBs containing the circuitry for the individual neuron populations should be stored in such a way that two things are avoided: falling and static electricity. The boards are reasonably durable, but every attempt should be made to not drop any of the circuit boards. If a board is dropped, all solder joints should be examined to ensure they have not broken. Static electricity can damage individual circuit elements and cause them to malfunction, ultimately requiring replacement of that part. This can be easily avoided when handling the boards by discharging any built up static charge prior to contact with the boards themselves.

The other area that requires some maintenance is the ribbon cable connector. Pins can be obstructed by residues, dust, or other debris, and sockets can be blocked by similar materials. Making sure these portions remain clean will allow for better signal transmission and acquisition. If manual cleaning is not sufficient, compressed air can dislodge obstructions. More serious obstructions or damage to the connector may require complete replacement in order to resolve any issues.

Power Supply

Accuracy from the DC voltage sources of the power supply are imperative for the neuron circuits to function properly. Ideally, prior to use, the outputs of the power supplies should be
verified to ensure that they are producing the desired voltage source. The contacts and sockets on the power supplies should also be kept clean to ensure that the wires connecting them to the rest of the system are able to function properly.

Any additional maintenance outlined in the information provided by the power supply manufacturer should also be adhered to in order to allow for optimal function.

**Function Generator**

Similar maintenance procedures should be followed for the function generator in regards to ensuring that the output signal is of the expected amplitude and phase. Again, clean contacts and sockets will allow for more accurate signal transmission and will improve the quality of data received.

Any additional maintenance outlined in the information provided by the function generator manufacturer should be adhered to in order to allow for optimal function.

**Oscilloscope**

As with the other devices in the testing setup, clean contacts and sockets are crucial for proper function of the oscilloscope. It is also advisable to ensure that the probes are functioning properly prior to gathering any sort of data. Malfunctioning probes should be replaced immediately.

Any additional maintenance outlined in the information provided by the oscilloscope generator manufacturer should be adhered to in order to allow for optimal function.
3 Technical Description

3.1 Dendrite

The dendrite is an iterative, passive circuit designed to filter the input signal of the neuron. Developing an unbranched dendrite system, such as the one used in the neuron circuits of this device, requires the use of a compartmental modeling approach, which provides a discrete approximation of the dendrite behavior popularized by cable theory. Fig. 17 shows the generic implementation of a single dendrite branch. The compartmental model more closely resembles cable behavior as the number of compartments used increases (i.e. the higher the value of n, the more physiologically realistic the dendrite model is). For the purposes of the implementation within this device, 10 compartments are used prior to the soma (n=9).

![Figure 17. A generic schematic for an unbranched dendrite is shown. The initial compartment (left) lacks an axial resistance as the signal immediately enters the dendrite, the intermediate compartment (iterated n times) exhibits axial resistance at both the beginning and end of the compartment, and the soma compartments (right) shows no axial resistance at all.]

Each dendrite compartment is made up of at most four different components. The axial resistance (R_a) represents the resistance encountered in the dendrite in relation to its function as a wire. This also separates the individual dendrite compartments. The membrane resistance (R_m) and membrane capacitance (C_m) help define the electrical behavior of the membrane in the dendrite, particularly its change in conductivity over time. This is done through the use of the membrane time constant (τ_m), which is defined in Equation 1.

\[ \tau_m = R_m C_m = R_M C_M \]

Equation 1: Determining the membrane time constant of a dendrite compartment.

This time constant determines the rate at which the dendrite “charges,” helping to determine the reactivity of the neuron its associated with. A smaller time constant results in a neuron with a faster response time. The final component is the battery representing the membrane’s resting potential (V_{rp}), which ultimately is used to add physiological realism to the dendrite. These component values may changed to model dendrites of different sizes, time constants, and resting potentials, even when going from compartment to compartment in the same dendrite.
In order to facilitate signal isolation between the dendrite and the axon, a current stop was implemented. This series of operational amplifier circuits, terminated by a diode, allows for the dendrite to function at physiological voltage levels, but also to create an appropriate input signal to the empirical axon model (see Fig. 18).

![Figure 18. The general schematic for the current stop is shown. R5 and R4 help to define the reactivity of the dendrite and determine the amplitude of the currents source to the axon.](image)

U5D (according to Fig. 18) represents a voltage follower op amp circuit that helps to isolate the incoming dendrite signal from the soma compartment. This is summed with the inverted (and potentially amplified) resting potential signal from U5A via the inverting summing amplifier of U5B. The resulting signal is an inversion of the original dendrite signal with the resting potential recalibrated to 0 mV. This then passes through a final inverting amplifier (U5C) where it is amplified to a point where it will stimulate the axon. The diode then acts as a final isolator. The voltage drop over the diode can be essentially ignored due to the scaling that is occurring throughout the currents stop.

The current stop also allows for the development of autonomously firing neurons. By increasing the magnitude of the resting potential signal (increasing R5), the axon can receive a signal that will always cause it to go above threshold. This results in the neuron firing until it is inhibited by some external source. This process generally requires some adjustment of R4 in order to achieve the desired scaling.

It is difficult to define any other steady state voltages in the dendrite system to the high variability and dependence on the input signal. The dendrite, when unaffected by any sort of stimuli, rests at $V_{RP}$, which in this model is set to approximately -60 mV. If signals are too strong in either the positive or negative direction, this problem will not be discernable until the current stop is reached, where the output voltage will be either +15V or -15V, based on the if the signal is excitatory or inhibitory, respectively.

### 3.2 Axon

The primary function of the axon unit is to generate an appropriate action potential train in response to the current injection provided by the dendritic response. The design is based upon the FitzHugh-Nagumo model for action potentials. This model is a simplification of the Hodgkin-Huxley model for action potentials and replaces the physiologically relevant ion channels with electronic current analogues. The design (see Fig. 19), provides a robust solution for simulating the different behaviors of each neuron population.
Figure 19. The schematic for a modified FitzHugh-Nagumo axon model. This model is used in all of the neuron populations implemented in the device.

While the FitzHugh-Nagumo provides a simplistic means for simulating neural axon behavior, its implementation comes by the sacrifice of realism. The current FHN model rests at 0 V and generates action potentials of 5 V in amplitude. These parameters differ greatly from physiological analogs, which typically rest at -60 mV with action potentials of approximately 100 mV in amplitude. As a result, a post-processing unit was implemented to correct output voltages to physiological levels by scaling and offset mechanisms. A circuit schematic of the axon post-processing unit can be seen below in Fig. 20.

Figure 20. The post-processing unit schematic for the axon. This series of op amp circuits scales the axon circuits signal in order for a physiologically realistic axon signal to be observed.

The post-processing unit of the axon consists of three non-precision operational amplifiers which work, in conjunction, to achieve both scaling and offset of the raw axon signal.
The operational amplifier labeled U6A functions as a voltage follower which eliminates the loading effects inherent in the system. The operational amplifier U6B functions as a summing amplifier with a scaling factor governed by the equation below. In this case, the output of the axon is summed with the resting potential source of -60 mV, using the appropriate scaling factors.

\[ V_{\text{out}} = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n} \right) \]

Equation 2. Determining the output voltage of an inverting summing amplifier.

Lastly, the operational amplifier labeled U6C functions as an inverter to revert the signal back to its correct orientation. The correction is needed to correct the normal function of the summing amplifier discussed above.

While this “stock” model functions properly for autonomously firing 1000 Hz neurons, some additional work is necessary to describe the desired physiologically accurate neuronal populations. To encompass all of the desired neural behaviors of each of these various populations, several modifications are necessary which directly impact the firing rate. These modifications include modifications to the axon itself, as well as modifications to the current stop of the dendrite. By manipulating the current stop of the dendrite, specifically R4 and R5 of Fig. 18, an artificial increase in resting potential can be achieved. For the R5 resistor, practical values range from 900 – 1.3 kΩ. For the R4 resistor, practical values range from 60k – 300 kΩ. From here, the neuron will exhibit profound changes in firing behavior at the cost of sacrificing physiological realism. Because the axon unit contains a post-processing unit, these changes can be artificially corrected for during observation.

Changes in the actual axon typically revolve around the C16 capacitor of Fig. 19. Changes in the capacitance of this value allow some manipulation of firing rate. For the C16 capacitor, typical values range from 20 – 200 nF. Together, these changes allow for a variable firing rate between 200 – 1300 Hz, depending on the input current pulse.

A comparison between the OPN and LLBN provides a perfect example of how these mechanisms can be used to manipulate firing rate and neural behavior. Refer to Table 3 below as a means of understanding the manipulation of the current stop.

<table>
<thead>
<tr>
<th>Property</th>
<th>LLBN</th>
<th>OPN</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>R$1$ Resistance of Current Stop</strong></td>
<td>1k Ω</td>
<td>1.26k Ω</td>
</tr>
<tr>
<td><strong>R$2$ Resistance of Current Stop</strong></td>
<td>300k Ω</td>
<td>61k Ω</td>
</tr>
<tr>
<td><strong>C$$ Capacitance of Axon Hillock</strong></td>
<td>60 nF</td>
<td>200 nF</td>
</tr>
<tr>
<td><strong>Resultant Frequency</strong></td>
<td>~1000 Hz</td>
<td>~250 Hz</td>
</tr>
<tr>
<td><strong>Autonomy?</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 3. A comparison of OPN and LLBN to illustrate frequency control.
3.3 Synapse

The synapse creates an output current that is proportional to the frequency of action potentials produced by the axon hillock. The first step is to create square pulses from action potentials in the presynaptic terminal, much like the release of neurotransmitter from vesicles when action potentials cause an influx of calcium ion. The presynaptic terminal circuitry is shown again for convenience in Fig. 21.

![Figure 21](image.png)

Figure 21. The comparator, left, and inverting amplifier, right, are shown.

The signal at the “Vin” pin on the comparator is the non-scaled action potential from the axon hillock. This output is of the comparator is given by equation A.

\[
V_{\text{out}} = \begin{cases} +V_{\text{supply}} & V_{\text{in}} > V_{\text{ref}} \\ -V_{\text{supply}} & V_{\text{in}} < V_{\text{ref}} \end{cases}
\]

Equation A. The output relationship for the comparator is given. In this case, \(+V_{\text{supply}} = 15V\), \(-V_{\text{supply}} = 0V\), and \(V_{\text{ref}} = 2V\).

A square pulse is generated that is roughly the width of an action potential, as seen in Fig. B.

The comparator output is fed to an inverting amplifier with a unity gain; the output is simply the inverse of the input. This inhibitory output is also shown in Fig. 22.

![Figure 22](image.png)

Figure 22. The input and outputs of the pre-synaptic terminal are shown. The input, in blue (bottom), is the unprocessed output from the axon hillock, and is shown with a scale of 5V/division and is shifted down three divisions for clarity. The excitatory output from the comparator is shown in green (top) with a scale of 10V/division and no shift. The inhibitory output is shown in red (middle) on the same scale as the excitatory output.
The use of the LMC6482AIM high-precision rail-to-rail operational amplifier ensures the output voltages reach the “rail” voltages of zero and ±15V. The use of a general-purpose operational amplifier, like the 741, would result in unreliable results because they saturate significantly before the output reaches the supply voltage.

Values in the pre-synaptic terminal need not be customized. An overview of operating voltages of the presynaptic terminal is given in Fig. 23.

![Figure 23](image)

Figure 23. An overview of operating voltage ranges of the presynaptic terminal is shown.

The generation of a postsynaptic potential is modeled as a summation of the inhibitory and excitatory voltages of the presynaptic neurons converted into a current that is injected into the postsynaptic dendrite. The circuit in Fig. 11 does this, and is again shown in Fig. 24.

![Figure 24](image)

Figure 24. The contents of the voltage summing and current block are shown, with the inverting summing amplifier indicated by the green rectangle (left), and the bilateral current source indicated by the blue rectangle (right).

The resistors of the summing amplifier may be manipulated to change its gain. Differing gain between multiple inputs can model the different synaptic strengths of neural inputs. The input-output relationship for the summing amplifier is given in Equation 3.

\[ V_{out} = -R_3 \left( \frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2} \right) \]

Equation 3. The relationship between output and input voltage for the summing amplifier is given.
The relative synaptic strengths are found largely by trial and error after seeing how parts of the system interact. The amplification of the bilateral current source may also be manipulated, but it is more convenient to only make changes to the summing amplifier. The bilateral current source relationship is given in Equation 4.

\[ I_{out} = -\frac{R_3 V_{in}}{R_1 R_5} \]

Equation 4. The relationship between output current and input voltage of the bilateral current source is given.

The following must also be true when adjusting the bilateral current source: \( R_3 \approx R_4 + R_5 \) and \( R_1 = R_2 \). The resistor values seen in Fig. 24 have already been selected such that \( I_{out}/V_{in} = -1 \cdot 10^{-4} \). It is also important to note that the sign of the current leaving the current source is opposite to that of the voltage at its input. Thus, a negative voltage at the output of the summing amplifier yields a current leaving the source, which is excitatory. The opposite is true for the positive voltage at the output of the summing amplifier.

Note the use once again of high-precision rail-to-rail operational amplifiers. The bilateral current source also calls for resistors with a 1% tolerance because of its precision.

In the configuration shown in Fig. 24, the operating voltages and currents are shown in Fig. 25. However, if adjustments are made to either amplifier, these values will change according to the relationships in equations 21 through 23.

![Figure 25](image.png)

Figure 25. The operating voltages and currents for this configuration of the voltage summing and current source block are shown.
4 Troubleshooting

Because the components of the neuron circuit boards are already soldered in place, part failure would most likely occur in a situation where the power sources are wired improperly. Failure to follow the power scheme can result in failure of all of the op amps in a very short time frame. If such a situation occurs, the behavior of all of the op amps can be checked via oscilloscope or multimeter. If any or all of them have failed, they will need to be replaced before any more simulations can be run.

4.1 Dendrite

The passive nature of the dendrite leaves it less prone to malfunctioning than the axon or synapse components, but also causes any problems that may arise to be harder to diagnose.

For the actual dendrite compartments, the most obvious sign that a problem has occurred is if the circuit is taking an abnormally long or short time to reach steady state. This would suggest that one of the parts, most likely a membrane resistor or capacitor, is defective and needs to be replaced. To identify the offending component, it is necessary to observe the individual compartments. This can be done via the use of an oscilloscope, or if necessary, a multimeter. By observing the rate of charging for each compartment, it is possible to see which compartment is not behaving in the expected manner. From here, testing the resistance of the components in that compartment should allow for the identification of the defective component. This should then be replaced before further simulations are run.

The current stop can have two major types of malfunctions occur. The first is related to the op amps, which are arguably the most likely part to fail in the dendrite. If an op amp fails, unusual amplification will be observed, causing unexpected firing rates from the axon or not allowing the axon to fire at all (whether due to an insufficient stimulus or via over-saturation). If such a scenario occurs, the LM348 op amp must be replaced, as all four op amp circuits work from the same chip.

The other potential issue would be diode failure. Though it is unlikely, the neuron will no longer be able to function if the diode fails. This is most easily observed by seeing current backflow into the current stop despite the diode’s presence. This can be resolved by replacing the diode.

4.2 Axon

In addition to op amp specific problems that may arise, the axon also has some unique complications that can occur from misuse. Specifically, the FHN axon is designed to only operate at certain current input ranges that are specific to the configuration and parameters designated by the previously discussed circuit components. This “ideal current injection interval” must be determined on a per neuron basis as it is a function of both the dendritic current stop and actual axon design. As a result, even small changes in neural configuration can have huge implications on the actual behavior of the axonal unit.

If configured improperly, one of two problems can arise. In the first, the axon will fire continuously, with dissipating amplitude. This problem arises when the current injection is higher than the sufficient operating interval. Minimization of current input or artificial decrease of resting potential is necessary to correct a problem of this result. On the other hand, in some cases the axon will never fire, despite an increase in dendrite voltage. This problem arises when the current injection is lower than sufficient operating interval. In a similar fashion, an increase of the current input or an artificial increase of resting potential is necessary to correct this problem.
4.3 Synapse

As with all operational amplifiers in the circuit, those in the synapse must also be checked for proper supply voltages. The second amplifier in Fig. 11, which is part of the current source, is the second on a dual chip, and is at risk for becoming disconnected with model changes. If this happens, there will be no current from the bilateral current source and the postsynaptic neuron will not be stimulated. Figure F shows this circuit in a nonfunctional condition.

Figure F. The voltage summing and current source circuit with missing power supplies on the rightmost amplifier. Note the lack of red Xs on pins 4 and 8.

The solution to the situation in Fig. F would be to replace U6B with another LMC6482AIM and when prompted, select part B of U3. This is illustrated in Fig. G.

Figure G. After replacing U6B with another LMC6482AIM, clicking the “B” button next to U3 will cause both amplifiers to be part of the same chip and be powered by the same supplies.

A second issue involves the comparator and inverter circuits. In this case, the operational amplifiers must be two separate chips so their supply voltages may be different. The comparator needs a zero and positive 15V supply, while the inverter needs ±15V. Using the same chip for the inverter as the comparator will result in no inhibitory output because there is no negative supply provided to the chip.

Though the solution to other problems in the circuit may lie in the synapse, this portion of the circuit should not give major trouble.